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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,863	AKKARY ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-22* is/are rejected.

7)☒ Claim(s) *14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been withdrawn.

2. Applicant's election with traverse of group II in the reply filed on 1/9/2006 is acknowledged. The traversal is on the ground(s) that no showing has been made as to the usability of the subcombinations. This is not found persuasive because group II has the utility of storing in a ***non-tagged*** array while group I has the utility of a tagged array since it includes speculative and valid bits (tags) with each cache block.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

a. ***a processor*** containing a ***logic to execute*** the at least one store operation and cause a queue to store a last n stores.

b. a circuit that contains an ***address matching circuit*** and a ***store select circuit***, which are adapted to forward stores and store data to any dependent loads

c. an circular n-entry buffer with head and tail pointers

d. a memory dependence predictor that stores store-distances in a non-tagged array

e. an unresolved address buffer adapted to determine a program order condition which includes whether or not non-issued load instructions are scheduled ahead of one or more store instructions

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 14 and 20 objected to because of the following informalities:

a. Relating to claims 14 and 20, the last line of each claim contains, "and/or" which is not appropriate as the store distance is between two things and when read "or" there is only one item and thus there cannot be a distance between it and nothing else.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 11-13, 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary et al., US patent 6591342 and Martinez et al., "Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors" (hereinafter Martinez).

9. With respect to claims 11, 17, Akkary teaches of a system comprising: a memory to store at least one store operation (column 1; lines 20-30; the processor reads the instructions from the software, it is abundantly clear to one of ordinary skill in the art that the instructions must be contained in a memory such as an instruction cache, RAM, or other memory);

a processor to retrieve the at least one store operation from the memory (column 1; lines 20-30, lines 32-34; the processor reads the instructions from the software, and store instructions are a part of the instructions),

the processor including logic to execute the at least one store operation (fig. 8; column 13, lines 1-11; as the processor executes the store operation, it must have logic to do such) and

cause a queue to store a last n stores (fig. 2; column 3, lines 42-60; as a store instruction enters the instruction window, an entry is allocated for it in the store queue. As this is done, there must be logic to do such); and

a circuit to receive and store non-retired stores from said queue (fig. 2, item 230; column 2, lines 45-49; column 4, lines 33-48; SFB is a set-associative buffer that stores store instruction information),

Akkary fails to explicitly teach of wherein said circuit includes at least one storage block to be associated with a checkpoint in a program.

However, Martinez teaches of wherein said circuit includes at least one storage block to be associated with a checkpoint in a program (p. 4, section 2.1; where the backup register file keeps the checkpointed register state).

Akkary and Martinez are analogous arts as they are both in the same field of endeavor, out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary and Martinez at the time of the invention to include the checkpoints by the backup register file keeping checkpointed register states in the SFB of Akkary as taught in Martinez. Their motivation would have been to allow the processor to roll back to a prior consistent state if needed (Martinez p. 4; section 2).

10. With respect to claims 12 and 18, Akkary teaches of wherein said circuit further comprises: an address matching circuit (fig. 2; column 1, lines 62-65; column 4, lines 49-55; as the SFB is searched for a store instruction upon which the load instruction depends, it must have address matching circuitry that compares the address with the store and load instructions); and

a store select circuit (column 7, line 66-column 8, line 5; column 9, lines 35-49; as only certain sets are searched in the SFB, there must be circuitry that selects the different store sets),

wherein both of said address matching circuit and said store select circuit forward stores and/or store data to any dependent loads (column 9, lines 35-49; where as a result of finding a matching entry, the store data is forwarded to the load instruction. It is abundantly clear to one of ordinary skill in the art that the circuitry used to search the SFB (address matching and selection circuitry) forwards the store data).

11. With respect to claims 13 and 19, Akkary fails to explicitly teach of wherein an n-entry buffer stores said queue, and wherein said n-entry buffer is a circular buffer with head and tail pointers.

However, Martinez teaches of wherein an n-entry buffer stores a queue, and wherein said n-entry buffer is a circular buffer with head and tail pointers (p. 2; figure 1).

Akkary and Martinez are analogous arts as they are both in the same field of endeavor, out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary and Martinez at the time of the invention to include a circular buffer with head and tail pointers in the SQ of Akkary storing the queue as taught in Martinez. Their motivation would have been to reduce the overhead required to maintain the data within the buffer.

12. Claims 14 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary and Martinez as applied to claims 11 and 17 respectively, and further in view of Jourdan, et al., US patent application publication 2003/0217251.

13. With respect to claims 14 and 20, the combination of Akkary and Martinez fails to explicitly teach of wherein said circuit further comprises a memory dependence predictor to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and/or forwarding store.

However, Jourdan teaches of wherein said circuit further comprises a memory dependence predictor to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and/or forwarding store (figs. 2, 4; paragraph 0020, 0023, 0024, 0032; as shown in figure 4, the array including the distance entries 400.1-400.k is not tagged).

The combination of Akkary and Martinez, and Jourdan are analogous arts as they are both related to out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez, and Jourdan at the time of the invention to include the dependence predictor in Jourdan into the SFB of the combination of Akkary and Martinez. Their motivation would have been to avoid executing instructions with invalid data and this having re-execute the instructions (Jourdan, paragraph 0002).

14. Claims 15 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary and Martinez as applied to claims 11 and 17 respectively, and further in view of Maier, et al., US patent application publication 2004/0044881.

15. With respect to claims 15 and 21, the combination of Akkary and Martinez fails to explicitly teach of said circuit further comprises an unresolved address buffer to

determine a program order condition, wherein said program order condition includes whether one or more non-issued load instructions are scheduled ahead of one or more associated store instructions.

However, Maier teaches of a circuit further comprises an unresolved address buffer to determine a program order condition, wherein said program order condition includes whether one or more non-issued load instructions are scheduled ahead of one or more associated store instructions (paragraph 0004; where in the special bypass buffer, the IDU compares instruction fields used for address generation of load instruction against store instructions. If a match is determined, it is speculated that the load instruction is dependent on the store instruction, and the address field of the store instruction is transferred to the load instruction. It is abundantly clear to one of ordinary skill in the art that this is done to avoid the potential of errors created having the dependent load instruction executing ahead of the store instruction).

The combination of Akkary and Martinez, and Maier are analogous arts as they are both related to out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez, and Maier at the time of the invention to include the special bypass buffer and process of speculating instruction dependency of unresolved instructions into the SFB of the combination of Akkary and Martinez. Their motivation would have been to reduce the complexity of control logic involved (Maier, paragraph 0003).

16. Claims 16 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary and Martinez as applied to claims 11 and 17 respectively, and further in view of Gopal, et al., "speculative versioning cache" (hereinafter Gopal).

17. With respect to claims 16 and 22, the combination of Akkary and Martinez fails to explicitly teach of wherein said circuit comprises: a speculative data cache.

However, Gopal teaches of wherein a circuit comprises a speculative data cache (fig. 5; p. 5, section 3.2).

The combination of Akkary and Martinez, and Gopal are analogous arts as they are both related to executing load and store operations. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez, and Gopal at the time of the invention to include the SVC of Gopal in the SFB of the combination of Akkary and Martinez. Their motivation would have been to enable a load or store to be speculatively executed before the address of all preceding loads and stores are known (Gopal, abstract).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER